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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TUCKER, WESLEY J	

ART UNIT	PAPER NUMBER
2623	12

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/749,819	FUKUDA ET AL.	
	Examiner	Art Unit	
	Wes Tucker	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3 and 6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The meaning of manifest image in claims 1, 6, and 11 is unclear and therefore renders the claims indefinite and confusing. Please clarify the meaning of manifest image in the context of the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,2,6,7,11,12 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,457,779 to Harrell.

With regard to claim 1, Harrell discloses an image processing apparatus comprising: an arithmetic processing unit (Fig.5, elements 401a - 401d) which

processes image data, being a digital signal prepared based on an image, as a manifest image, said arithmetic processing unit including,

an arithmetic processing section (Fig.5, element 410) of SIMD (Single Instruction Multiple Data stream) type that can process a plurality of image data at the same time (column 17, lines18-24). In Figure 5, element 410 is an arithmetic logic unit and each processor 401a – 401d has its own arithmetic logic unit enabling SIMD operation.

a plurality of memories (Fig.5, elements 701a-701d and Fig.6, elements 701a-701d) connected to said arithmetic processing section (Fig.5, element 410); and a memory controller (Fig.6, element 700a) which controls each of said memories,

wherein said memory controller controls transfer of image data performed between said memory and said arithmetic processing section (column 17, lines 60-65 and column 18, lines 12-15). Here a cross point circuit (Fig.6, element 705) is explained as part of the indirection circuit (Fig.6, element 700a). The cross point circuit operates with combinational logic circuit (Fig.6, element 710) as a part of the indirection circuit or memory controller and controls the data transfer between the memories and mathematical unit (Fig. 5, element 410) or arithmetic processing section.

With regard to claim 2, Harrell discloses the image processing apparatus according to claim 1, wherein said memory controller (Fig. 6, 700a) is connected to a control register (Fig.6, element 710), and said control register has a data transfer mode setting function (Fig.6, element 712) for setting the data transfer mode of the memory connected to the memory controller. The combinational logic element 710 determines

how data is transferred from memory 701a-d to the mathematical unit 410 via the cross point circuit 705. The combinational logic element 710, which is part of the memory control also has a selection mode element 712 that selects the mode in which the data from memory will be transferred (column 21, lines 7-13).

Claims 6 and 7 are similar to claims 1 and 2 except that 6 and 7 make reference to means. It is understood that means is included in the elements such as registers, controllers, units, etc. Therefor the discussions of claims 1 and 2 apply for claims 6 and 7.

Claims 11 and 12 are similar to claims 1 and 2 except that 11 and 12 make reference to method. It is understood that the intended method is included in the apparatus claimed in claims 1 and 2. Therefore the discussions of claims 1 and 2 apply for claims 11 and 12

With regard to claim 16, Harrell discloses A computer readable medium for storing instructions (column 10, lines 15-20), which when executed by a computer, causes the computer to perform an image processing method to be executed by an image processing apparatus, said image processing apparatus including an SIMD type arithmetic processing section for processing a plurality of image data (Fig.5, element 410), being digital signals prepared based on an image, at the same time; a plurality of memories (Fig. 6, elements 701a-701d) connected to said arithmetic processing

section; and a memory controller (Fig.6, element 700a) for controlling each of said memories, the method comprising:

an image data control step for controlling transfer of image data, performed between said memory and said arithmetic processing section, by said memory controller (column 21, lines 7-13). See also discussion for claims 1 and 2.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3,4,8,9,13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of U.S. Patent 5,457,779 to Harrell and U.S. Patent 5,729,503 to Manning.

With regard to claim 3, Harrell discloses the image processing apparatus according to claim 2, but does not disclose a controller register that changes over setting of a random access mode in which an access is set to access the memory, and setting of an automatic access mode in which an address is automatically updated to access the memory, in accordance with a control signal provided from outside.

Manning discloses a controller register that changes depending on the memory access setting (column 11, lines 9-15). Here a multiplexer is described to select

between a page mode and a burst mode of memory access. The multiplexer is the acting memory controller containing a register that changes according to the memory access mode in this embodiment. The page mode memory access is equivalent to an automatic access mode in which an address is automatically updated to access the memory, and the burst mode is equivalent to the random access mode in which an address is set to access the memory. The burst mode and page mode are described in column 3, lines 3-23. A memory controller is also described in another embodiment of the invention that selects between burst and page transfer modes (column 11, lines 35-55). The control signal for choosing the transfer mode comes from outside and is represented by control signal lines 116 (column 11, lines 37-40) or in the case where the multiplexer acts as the memory controller, the multiplexer select is the outside signal (column 11, lines 13-15).

Manning teaches that these memory access modes are used for high speed data access and for compatibility with existing memory systems (column 2, lines 53-55). Manning gives more details on the advantages of using these kinds of memory access modes in column 3, lines 10-23. When accessing memory for a great amount of data such as in image processing speed is very advantageous. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to employ the memory access modes of Manning in order to provide increased speed in processing large amounts of image data.

With regard to claim 4, Harrell discloses the image processing apparatus according to claim 2. Harrell does not disclose an apparatus wherein said control register reads data redundantly from said memory, in accordance with a control signal provided from outside, and sets a redundant readout transfer mode for transferring data to said arithmetic processing section. Manning discloses reading data redundantly (column 11, lines 60-65). Here reading data redundantly is interpreted as reading data from two different sources. Manning refers to reading data from the SRAM cache in addition to the memory. It is understood that a redundant transfer mode would have to be set in the memory controller register.

Manning teaches that the advantage of reading data redundantly or from two sources is that it yields a higher performance computer design by providing fast access to main memory in the event of a cache miss. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use redundant memory data readout employed by Manning in order to produce a higher performance computer by providing fast access to memory.

With regard to claims 8 and 13, the discussion of claim 3 applies. With regard to claims 9 and 14, the discussion of claim 4 applies.

Claims 5,10, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of U.S. Patent 5,457,779 to Harrell and U.S. Patent 6,229,954 to Yamagami et al.

With regard to claim 5, Harrell discloses the image processing apparatus according to claim 2, but does not disclose the apparatus wherein said control register reads data from said arithmetic processing section by thinning out, in accordance with a control signal provided from outside, and sets a thinning-out read transfer mode for transferring data to said memory. Yamagami discloses a thinning out process (column 4, lines 15-25). Here a thinning-out process circuit (Fig.2, element 204) is disclosed and is controlled by the bus controller (Fig.2, element 206) which controls the data transfer between memory and the thinning out circuit and is therefore the memory control. The bus controller receives an outside signal from the External I/F Controller (Fig.2, element 207) and sets the data transfer to thinning-out. Thinning-out of data in a digital image environment is useful because memory is limited and digital images contain a relatively large amount of data. Any thinning out or minimization of data needed to represent the digital image will result in more available memory to be used. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use the thinning out technique of Yamagami in order to better utilize limited memory in the enviroment of digital imaging.

With regard to claims 10 and 15, the discussion of claim 5 applies.

The prior art made of record but not relied upon is considered pertinent to the applicant's disclosure.

U.S. Patent 6,032,234 to Kishi discloses a clustered multiprocessor system with multiple memories.

U.S. Patent 6,038,350 to Iwase et al. discloses a signal processing apparatus with multiple memories and ALUs.

U.S. Patent 6,052,129 to Fowler et al. discloses a method and apparatus for image processing containing multiple memories, arithmetic unit, and a memory controller.

U.S. Patent 6,049,859 to Gliese et al. discloses a matrix array of processor units with memories and ALUs.

U.S. Patent 5,151,881 to Kajigayaet al. discloses multiple memory address access modes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wes Tucker whose telephone number is 703-305-6700. The examiner can normally be reached on 9AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amelia Au can be reached on (703)308-6604. The fax phone number for the organization where this application or proceeding is assigned is (703)308-5397.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Wes Tucker
11-26-03

Jon Chang
Primary Examiner